Official

Attorney's Docket No.:10559-348001

7/7/03

In the Claims:

Please cancel claims 15 and 16, as reflected below, without prejudice or disclaimer.

Claim 1. (Original) A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

Claim 2. (Original) The method of claim 1, wherein said providing said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface.

Claim 3. (Original) The method of claim 2, wherein an operating voltage level of said first sub-interface is less than 1.0 volt.

Claim 4. (Original) The method of claim 2, wherein an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

Claim 5. (Original) The method of claim 1, wherein said providing said at least one buffer isolates the first and second

11

sub-interfaces in such a manner that the first sub-interface is operated at higher frequency than the second sub-interface.

Claim 6. (Original) The method of claim 5, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

Claim 7. (Original) The method of claim 6, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

Claim 8. (Original) The method of claim 1, wherein said at least one buffer are provided on a same memory board as the memory modules corresponding to said at least one buffer.

Claim 9. (Original) The method of claim 1, wherein said chipset is provided on a motherboard.

Claim 10. (Original) The method of claim 1, wherein said interface between the chipset and the memory modules is a multidrop bus.

Claim 11. (Original) The method of claim 1, wherein each of said memory modules includes dynamic random access memory (DRAM).

Claim 12. (Original) The method of claim 1, wherein each of said memory modules includes double data rate (DDR) DRAM.

Claim 13. (Original) The method of claim 1, wherein each of said memory modules includes quad data rate (QDR) DRAM.

Claim 14. (Original) A method, comprising:

providing at least one buffer in an interface between a chipset and memory modules, said at least one buffer allowing

the interface to be split into first and second sub-interfaces, where the first sub-interface is between the chipset and the at least one buffer, and the second sub-interface is between the at least one buffer and the memory modules, said at least one buffer isolates the first and second sub-interfaces in such a manner that the first sub-interface is operated at different voltage level than the second sub-interface, and the first sub-interface is operated at higher frequency than the second sub-interface; and

configuring said at least one buffer to properly latch the data being transferred between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other.

Claim 15. (Canceled)

Claim 16. (Canceled)

Claim 15. (Original) A method, comprising:

isolating a memory interface between a chipset and memory modules, where said isolating divides the memory interface into first and second sub-interfaces; and

configuring said first and second sub-interfaces to properly transfer data between the chipset and the memory modules, such that the first and second sub-interfaces operate independently but in synchronization with each other,

wherein said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

Claim 16. (Original) The method of claim 15, wherein an operating voltage level of said first sub-interface is less than

1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

Claim 17. (Original) The method of claim 15, wherein said first sub-interface is operated at twice the frequency of the second sub-interface, and a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.

Claim 18. (Original) A system, comprising:

a memory interface between a chipset and at least one memory module; and

at least one buffer disposed in said memory interface to divide said memory interface into first and second sub-interfaces,

where said first and second sub-interfaces are configured in such a manner that the first sub-interface is operated at different voltage level and at higher frequency than the second sub-interface.

Claim 19. (Original) The system of claim 18, wherein an operating voltage level of said first sub-interface is less than 1.0 volt, and an operating voltage level of said second sub-interface is between 1.2 and 1.8 volts.

Claim 20. (Original) The system of claim 18, wherein said first sub-interface is operated at twice the frequency of the second sub-interface.

Claim 21. (Original) The system of claim 20, wherein a number of data lines in said first sub-interface is half that of a number of data lines in said second sub-interface.